SDIF Converter — SS–612

User Manual

Rev. 3

Introduction

The SS–612 SDIF Converter performs simultaneous bidirectional conversion between the Sony Digital Interface (SDIF–2) and AES3/IEC 958 digital audio formats. The device cannot generate a clock but can recover a clock signal from either AES or SDIF.

Installation

The device may used directly or mounted in a 19 inch EIA type rack adapter. If the unit is going to stand alone, four self–adhesive rubber feet are provided. If the rack adapter is used, do not apply the rubber feet or they will interfere with installation.

Install the SDIF Converter in the rack adapter by sliding the unit into the front of the adapter. Align the four holes on the adapter with the four holes on the top and bottom of the SDIF Converter case. Four #4 screws are provided with the rack adapter to fasten the case to the adapter. The rack adapter can hold two half rack units. If a single Converter is mounted in the adapter, use of the accompanying filler panel is recommended. The filler panel provides rigidity when the rack adapter is only partially filled.

♦ Power

The SDIF Converter has a standard IEC power connector. The user must manually select for either 110 or 220 Volt (V) service. To do this, disconnect the power cord and remove the fuse tray and voltage selector. Rotate the voltage selector to the desired setting and reinstalling the voltage selector, fuse drawer and power cord. The unit will function with 90V to 240V service at 50 or 60 Hz.

The fuse drawer contains two fuses. Both fuses are 0.5A, 250V, 5 x 20mm fuses. If you suspect fuse failure, check both fuse locations. When power is applied to the Converter, the light emitting diode (LED) on the far left should glow green. Since there is no power switch, the unit begins functioning when power is applied.

♦ Optical Connectors

The RCZ–6901 optical connections conform to the IEC–958 specification. They can drive 10 meters of plastic fiber cable. The female connectors are shipped with dust covers inserted into the optical receptacle. These dust covers protect the optical hardware during manufacture and shipping. They must be removed before attaching optical cables and should be replaced when a receptacle is not in use. Optical male cable assemblies also ship with dust covers. The same recommendations apply.

♦ SDIF Connectors

Six BNC type connectors on the back of the case provide the SDIF interface. When the Converter derives its clock from SDIF, a Word Sync input (WS IN) must be connected. WS IN need not be connected if the unit's clock source is AES. Remember to never connect WS IN to WS OUT. This will cause a clock loop and the Converter will not function properly.

☞ Note that the Word Sync input is not internally terminated. If the Word Sync input is used, it *must* be terminated with a 75 Ω load. To accomplish this, attach a BNC Tee (T) connector to the WS IN port. Plug the coaxial cable with incoming Word Sync into one "arm" of the Tee and a 75 Ω BNC–style terminating resistor into the other arm of the Tee.

Front Panel Operation

There are five LEDs and one toggle switch on the front panel that are used during normal operation. The Clock source switch sets which "side" of the interface, either SDIF or AES, will serve as the source for clock. The two lock LED's show that clock is being received from their respective interfaces. AES lock indicates that an internal phase locked loop (PLL) is locked to the incoming optical data stream. This PLL is designed to lock to sample rates from 44.1 kHz to 48 kHz. The SDIF Lock LED indicates that an internal PLL is locked to WS IN. This PLL can also lock to sample rates from 44.1 kHz to 48 kHz. Neither of these LEDs show that valid data is being received. They only indicate that clock is being recovered.

The unit attempts to intelligently select the clock source. If only one side of the interface is receiving valid clock, then the clock source switch setting is ignored and clock is taken from the locked side of the interface. If both sides of the interface are phase locked, the switch will designate the side of the interface that provides clock.

The two red LEDs check the data integrity of their respective incoming data streams. AES Error LED shows that either an invalid bit or parity errors exist in the AES data stream. The SDIF Error LED shows that the incoming SDIF data does not contain valid blocking information. SDIF sends a special indicator every 256 samples signaling the start of a new data block. If the blocking information does not arrive or arrives at the wrong time on either channel, the SDIF error LED will be lit. SDIF doesn't really have any data integrity information in its data stream (CRC, parity, etc.). The SDIF error circuitry should be not used as a definitive or final arbiter of valid data.

Conversion details

SDIF and AES differ in several areas. This sections covers the caveats of converting from one format to the other. The only status information SDIF carries are emphasis flags for channels 1 and 2. These flags are stored and passed through as emphasis flags in the channel status flags of AES. SDIF blocking occurs every 256 samples and AES blocking every 192 samples and the blocks are not aligned between AES and SDIF, a change in the emphasis flag in the SDIF stream may not be reflected in the AES stream until many samples later. The delay will not exceed two SDIF blocks. The only channel status

information extracted from the AES stream is the emphasis flag for channels A and B. This flag is retransmitted in the SDIF data stream with a maximum delay of 2 SDIF blocks.

Other than emphasis, channel status information in the generated AES data stream is determined by the front panel DIP switch settings. See the following section on advanced use.

If the Converter is receiving its clock from SDIF, the WS IN connector must provide the clock source. Some SDIF equipment derives clock from CH1 or CH2, but this box requires a WS input to derive clock from SDIF.

Advanced Use

The front panel has ten DIP switches for configuring AES channel status and other details of the data streams. Changing these switch settings requires detailed technical knowledge and an oscilloscope if they are to be changed from their default positions. The switches and their default settings are shown in the figure below:

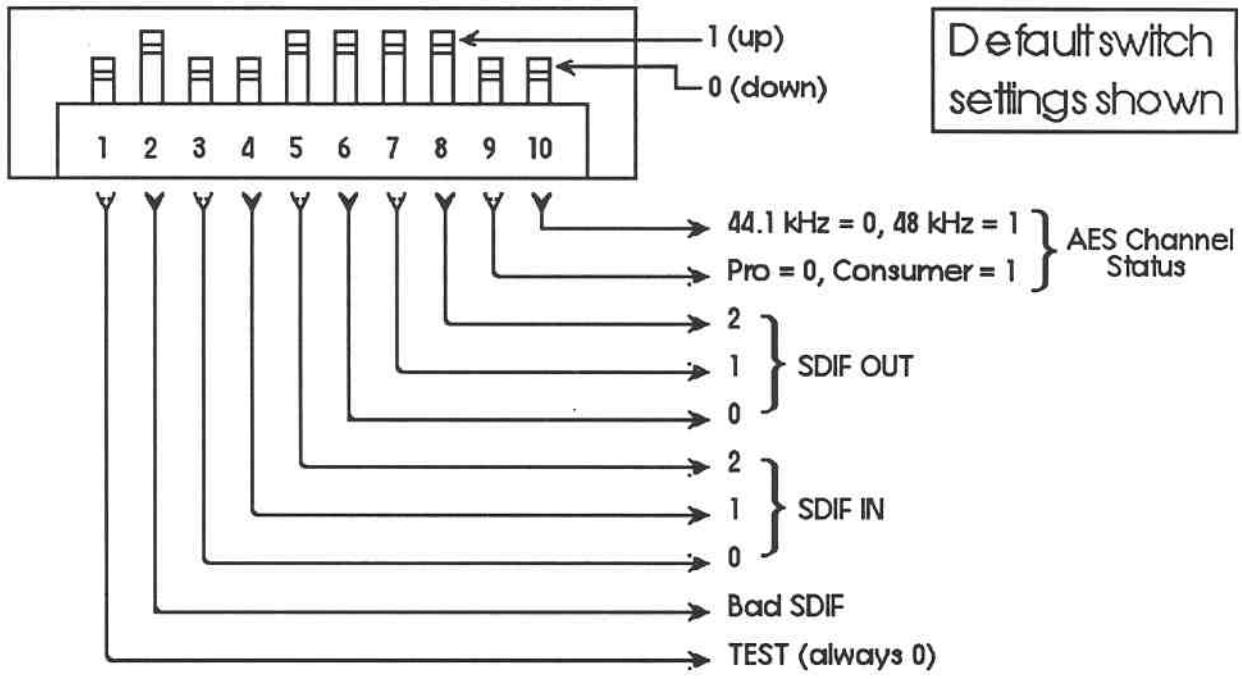

Figure 1: Front panel DIP switch settings & function

The switches are used as follows:

TEST

This bit is for testing in the factory and should be left in the zero or down position.

BAD SDIF

This bit decides what should be done with received SDIF data when the SDIF Error light is on. If set to 1 and if the error light is on, the Converter transmits zeros out of the AES interface. If set to 0, data is converted to AES even if it is assumed to be in error. This setting accommodates certain types of SDIF equipment that does not transmit standard blocking information but still transmits valid data.

PRO/CON

This bit configures the channel status bits for equipment class. A setting of 0 means "professional" and 1 means "consumer." When in consumer mode, the copy protection bit is always set to allow copying.

44.1/48

This bit sets the sample rate bits in the generated AES stream for 44.1 or 48 kHz sampling rates. For some devices, such as consumer DAT machines, this switch must be set correctly by the user for the DAT machine to respond to the AES data. For details on channel status bit combinations that can be transmitted, see Figure 1. For more detailed information on Channel Status, see Appendix 4 of the Sonic System User Manual.

SDIF OUT

These bits allow the user to set the phase relationship between word sync and the generated SDIF data. The position of the data bits relative to word sync may be moved in 1/8 bit time increments. This feature accommodates certain types of SDIF equipment that are very particular about the relative position of data bits. These bits avoid using a lengthy word sync cable to introduce a time delay in the word sync data relative to the audio data. Figure 2 shows the settings of these bits and the resulting bit position relative to word sync. Do not change these switch setting without prior forethought and proper test equipment.

SDIF IN

These bits allow the user to set the sampling point of the incoming SDIF data relative to word sync. This fits some types of SDIF equipment that might have an unusual phase relationships between data and word sync. Figure 3 shows the SDIF data sampling point relative to word sync. Do not change these switch setting without prior forethought and proper test equipment.

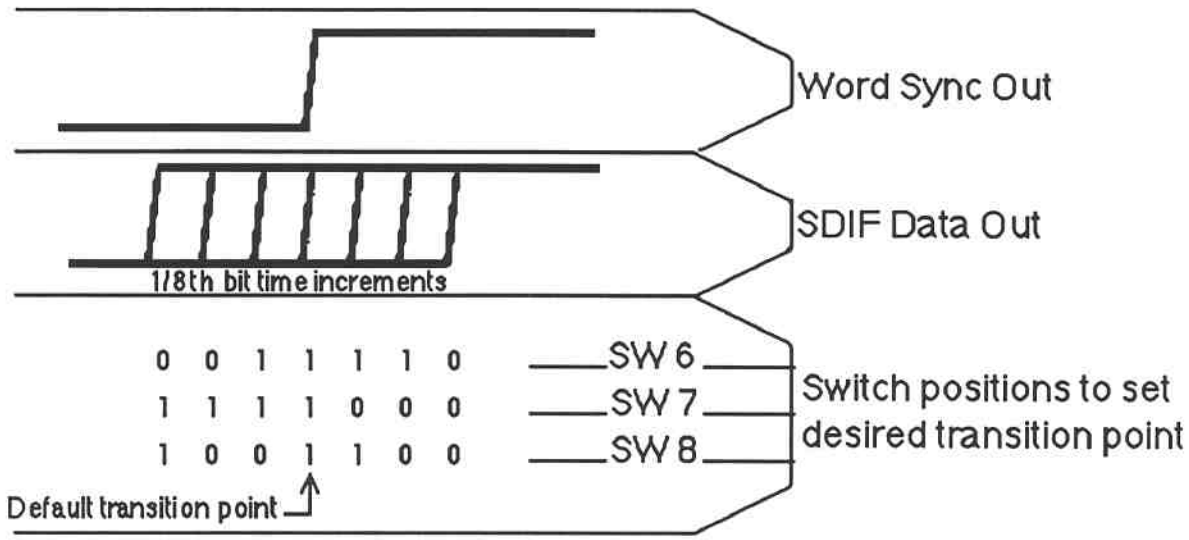

Figure 2: SDIF data output relative to word sync

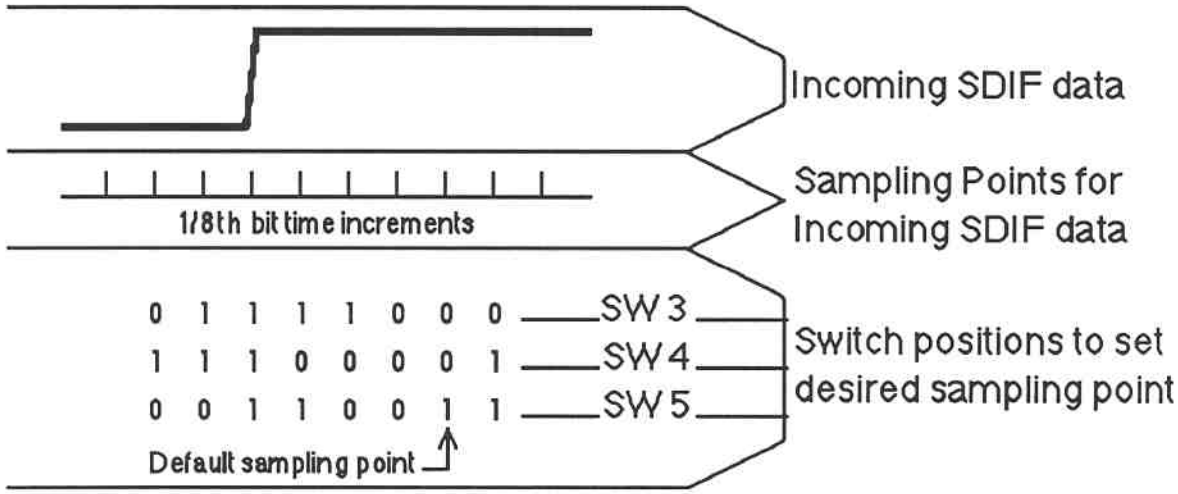

Figure 3: SDIF data sampling point relative to word sync

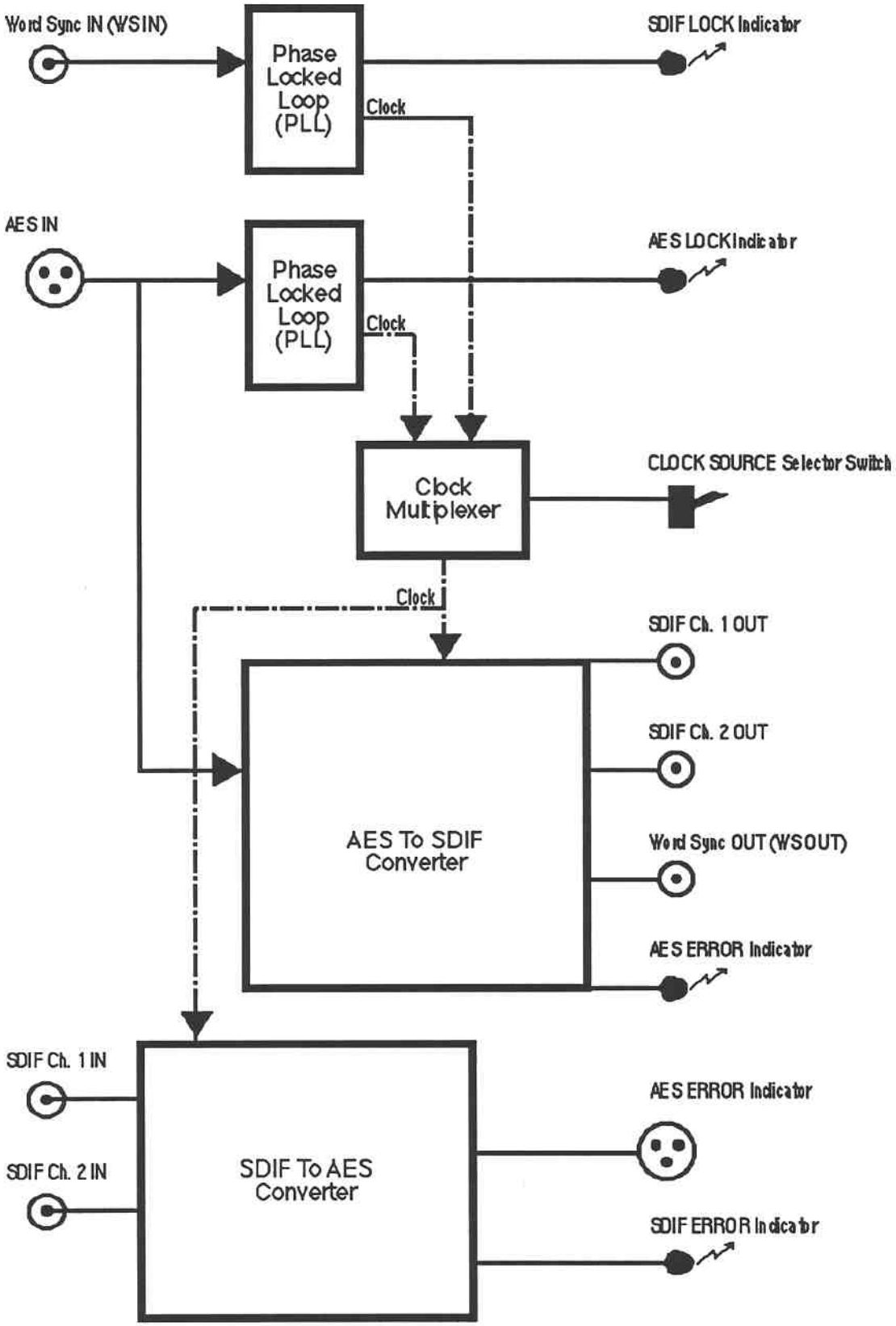

Figure 4: SDIF Converter block diagram